Roll No. | | | | | | | | | | | | | **Total No. of Pages : 02**

Total No. of Questions : 18

B.Tech.(ECE) (2018 Batch) (Sem.–3)

DIGITAL SYSTEM DESIGN

Subject Code : BTEC-302-18

M.Code : 76445

Time : 3 Hrs. **Max. Marks : 60**

INSTRUCTIONS TO CANDIDATES :

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION-A

Write briefly :

1) Convert decimal number 37.125 to octal number system.

2) State De-Morgan's theorem.

3) Draw full adder circuit diagram.

4) What is the purpose of select lines in multiplexer?

5) Draw and explain Latch.

6) What do you mean by FSM?

7) What are the limitations of weighted resistor DAC?

8) Explain FPGA.

9) What are the disadvantages of data flow modelling?

10) Write various data types in VHDL.

SECTION-B

11) Solve the following Boolean function using 8:1 multiplexer :

$F = \sum m(0, 1, 2, 3, 5, 7, 8, 9, 10, 11, 13, 15)$

12) Add decimal numbers 34 and 25 using BCD adder.

13) What is race around condition and how can we avoid it?

14) Draw and explain dual slope ADC.

15) Write a VHDL code for binary to grey code converter.

SECTION-C

16) Draw and explain various types of TTL logic family.

17) Design Logic gates AND, OR, NOT, X-OR, X-NOR using NOR gates only.

18) Explain universal shift register.

NOTE : Disclosure of Identity by writing Mobile No. or Making of passing request on any page of Answer Sheet will lead to UMC against the Student.