Roll No.
Total No. of Pages : 02
Total No. of Questions : 08
BCA (Sem.-2)
COMPUTER SYSTEM ARCHITECTURE
Subject Code : UGCA-1908
M.Code : 77416

Date of Examination : 12-08-21
Time: 2 Hrs.
Max. Marks: 60

## INSTRUCTIONS TO CANDIDATES :

1. Attempt any FIVE question(s), each question carries $\mathbf{1 2}$ marks.
2. Simplify F together with don't care conditions $d$ in (i) SOP (ii) POS for m .
$\mathrm{F}(w, x, y, z)=\sum(1,2,8,9,12,13), d(w, x, y, z)=\sum(10,11,14,15)$
Solve the following Boolean functions :
a) $x y+x y^{\prime}$
b) $(x+y)\left(x+y^{\prime}\right)$
c) $x z+x y z^{\prime}$
d) $(a+b)^{\prime}\left(a^{\prime}+b^{\prime}\right)$
3. a) The functionality of a 2 to 4 line decoder is presented in the table below :

| Inputs |  |  |  | Outputs |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A1 | A0 | EN | S3 | S2 | S1 | S0 |  |
| X | X | 0 | 0 | 0 | 0 | 0 |  |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 |  |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 |  |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 |  |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 |  |

b) What are the minimum sum-of-products equations for each output of the 2-to-4 line decoder?
3. a) Represent the decimal number 8620 in
a. BCD
b. Excess-3
c. 8421 code
d. as a binary number.
b) Explain the conversion of an expression from SOP form to POS.
4. Explain the working of full adder with the help of truth-table, logic diagram and addition operation table.
5. A computer uses a memory unit of 256 K words of 32 -bit each. Binary-instruction code is stored in one word of memory. The instruction has four parts an I bit, an operation code, a register codes part to specify one of the 64 registers and an address part:
a) How many bits are there in the operation code, the register code part and the address part?
b) Draw the instruction word format and indicate the number of bits in each part.
c) How many bits are there in data and address inputs of memory?
6. How will the computer system identify MRI, non-MRI and register reference instructions? What is the difference in the nature of these? Explain.
7. An arithmetic circuit has two selection variables $\mathrm{s}_{1}$ and $\mathrm{s}_{0}$. The arithmetic operations available have been listed below. The circuit must be incorporated with a full-adder in each stage of the arithmetic unit :

| S1 | S0 | $\mathbf{C 1}=\mathbf{0}$ | $\mathbf{C 1}=\mathbf{1}$ |
| :--- | :--- | :--- | :--- |
| 0 | 0 | $\mathrm{~F}=\mathrm{A}+\mathrm{B}$ | $\mathrm{F}=\mathrm{A}+\mathrm{B}+!$ |
| 0 | 1 | $\mathrm{~F}=\mathrm{A}$ | $\mathrm{F}=\mathrm{A}+!$ |
| 1 | 0 | $\mathrm{~F}=\mathrm{B}^{\prime}$ | $\mathrm{F}=\mathrm{B}^{\prime}+!$ |
| 1 | 1 | $\mathrm{~F}=\mathrm{A}+\mathrm{B}^{\prime}$ | $\mathrm{F}=\mathrm{A}+\mathrm{B}^{\prime}+!$ |

8. Describe the need of a multiplexer in a system. How is a multiplexer different from a decoder? Draw the logic diagram of $8 \times 1$ multiplexer and $2 \times 4$ decoder.

Note: Any student found attempting answer sheet from any other person(s), using incriminating material or involved in any wrong activity reported by evaluator shall be treated under UMC provisions.
Student found sharing the question paper(s)/answer sheet on digital media or with any other person or any organization/institution shall also be treated under UMC.
Any student found making any change/addition/modification in contents of scanned copy of answer sheet and original answer sheet, shall be covered under UMC provisions.

