Roll No. [ ][ ][ ][ ][ ][ ][ ][ ][ ][ ][ ]                Total No. of Pages: 02

Total No. of Questions: 07

**BCA (2011 & Onward)   (Sem. – 3)**
# DIGITAL CIRCUITS AND LOGIC DESIGN
**M Code: 10059**
**Subject Code: BSBC-303**
**Paper ID: [B0230]**

Time: 3 Hrs.                                                Max. Marks: 60

**INSTRUCTIONS TO CANDIDATES:**
1.   SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.
2.   SECTION-B contains SIX questions carrying TEN marks each and students have to attempt any FOUR questions.

## SECTION A

1.  a)   What is 1's and 2's complement?

    b)   What is Universal Gate?

    c)   What is Use of K-Maps?

    d)   Draw circuit of Full Adder with truth table.

    e)   What is limitation of R-S Flip-Flop?

    f)   What is limitation of J-K Flip-Flop?

    g)   What is clock?

    h)   What is a counter?

    i)   Draw AND gate using NOR Gate and Justify through truth table.

    j)   Fill in the Blank: $(25.75)_{10} = (?)_2$

## SECTION B

2. Complete the following table:

| Hexadecimal | Decimal | Octal | Binary |
|---|---|---|---|
| ? | ? | ? | 100000110 |
| ? | ? | 602 | ? |
| ? | 173.5 | ? | ? |
| CF3 | ? | ? | ? |

3. a) Use two 2-4 line decoders to make a 3-8 line decoder and explain its working.

   b) Explain the working of T flip-flop and D flip-flop.

4. Draw and explain the working of 4-bit binary adder-subtractor.

5. Discuss 555 timer as Monostable and Multivibrator.

6. What are Up-Down Counters? Explain the working of any Up-Down counter.

7. Explain how a master-slave J-K Flip-Flop can avoid race condition?